UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,494	02/06/2002	Taeg-Hyun Kang	40013.001	1924

27966 7590 12/19/2002

KENNETH E. HORTON
RADER, FISHMAN & GRAUER PLLC
RIVERPARK CORPORATE CENTER ONE
10653 SOUTH RIVERFRONT PARKWAY, SUITE 150
SOUTH JORDAN, UT 84095

EXAMINER	
MANDALA, VICTOR A	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/071,494	Applicant(s) KANG ET AL.	
	Examiner Victor A Mandala Jr.	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) *11-18 and 30-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,19-29,40 and 41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Examiner has noted that the applicant has responded to the election restriction from the last communication response. The applicant has elected the device claims 1-10, 19-29, and 40-41 for further examination with traverse. Examiner has considered applicants' arguments and makes election of device claims final.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the n type substrate as claimed in claim 3 and the field effect transistor that has no gate insulator as claimed in claims 40 and 41 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 40 and 41 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The invention shows a gate insulator and the disclosure discloses a gate insulator, but the claims 40 and 41 are teaching the invention without a gate insulator.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 19, 27, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,623,154 Murakami et al.

4. Referring to claim 1, a field transistor comprising: a well region of a first conductivity type, (Figure 1 #20); a field oxide layer, (Figure 1 #15), for defining an active region, (Figure 1 area of #20), on the well region, (Figure 1 #20); high concentration source and drain regions of a

second conductivity type, (Figure 1 #9), separated from each other by a width of the field oxide layer, (Figure 1 #15); a low concentration source region of the second conductivity type, (Figure 1 #7), formed in the well region, (Figure 1 #20), the low concentration source, (Figure 1 #7), region being adjacent to the high concentration source region, (Figure 1 #9), and overlapped by one end of the field oxide layer, (Figure 1 #15); a low concentration drain region of the second conductivity type, (Figure 1 #7), formed in the well region, (Figure 1 #20), the low concentration drain region, (Figure 1 #7), being adjacent to the high concentration drain region, (Figure 1 #9), and overlapped by the other end of the field oxide layer, (Figure 1 #15); and a gate conductive layer pattern formed on the field oxide layer, (Figure 1 #15), the gate conductive layer pattern, (Figure 1 #17), overlapping parts of the low concentration source and drain regions of the second conductivity type, (Figure 1 #7).

5. Referring to claim 19, a semiconductor device, comprising: a substrate, (Murakami et al. Figure 1 #1), comprising a well region of a first conductivity type, (Murakami et al. Figure 1 #20); a field oxide layer, (Murakami et al. Figure 1 #15), located over a portion of the well region, (Murakami et al. Figure 1 #20); a first source region of a second conductivity type, (Murakami et al. Figure 1 #9), and a first drain region of a second conductivity type, (Murakami et al. Figure 1 #9), separated by the field oxide layer, (Murakami et al. Figure 1 #15); a second source region having a second conductivity type concentration lower, (Murakami et al. Figure 1 #7), than the first source region, (Murakami et al. Figure 1 #9), the second source region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first source region, (Murakami et al. Figure 1 #9), with a portion of the second source region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al.

Figure 1 #15); a second drain region having a second conductivity type concentration lower, (Murakami et al. Figure 1 #7), than the first drain region, (Murakami et al. Figure 1 #9), the second drain region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first drain region, (Murakami et al. Figure 1 #9), with a portion of the second drain region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); and a conductive layer, (Murakami et al. Figure 1 #17), formed over the field oxide layer, (Murakami et al. Figure 1 #15), the conductive layer, (Murakami et al. Figure 1 #17), overlapping the second source region, (Murakami et al. Figure 1 #7), and the second drain region, (Murakami et al. Figure 1 #7).

6. Referring to claim 27, a semiconductor device comprising: a substrate, (Murakami et al. Figure 1 #1), comprising a well region of a first conductivity type, (Murakami et al. Figure 1 #20); a field oxide layer, (Murakami et al. Figure 1 #15), located over the well region, (Murakami et al. Figure 1 #20); a first source region of a second conductivity type, (Murakami et al. Figure 1 #9), and a first drain region of a second conductivity type, (Murakami et al. Figure 1 #9), separated by the field oxide layer, (Murakami et al. Figure 1 #15); a second source region having a second conductivity type, (Murakami et al. Figure 1 #7), concentration lower than the first source region, (Murakami et al. Figure 1 #9), the second source region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first source region, (Murakami et al. Figure 1 #9), with a portion of the second source region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); a second drain region having a second conductivity type, (Murakami et al. Figure 1 #7), concentration lower than the first drain region, (Murakami et al. Figure 1 #9), the second drain region, (Murakami et

al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first drain region, (Murakami et al. Figure 1 #9), with a portion of the second drain region underlying the field oxide layer, (Murakami et al. Figure 1 #15); a conductive layer formed over the field oxide layer, (Murakami et al. Figure 1 #15), the conductive layer, (Murakami et al. Figure 1 #17), overlapping the second source region, (Murakami et al. Figure 1 #7), and the second drain region, (Murakami et al. Figure 1 #7); a gate electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the conductive layer, (Murakami et al. Figure 1 #17); a source electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the first source region, (Murakami et al. Figure 1 #9); and a drain electrode, (It is apparent there would be an electrode in order for the device to work), electrically connected to the first drain region, (Murakami et al. Figure 1 #9).

7. Referring to claim 29, a system for electrostatic discharge protection containing a field transistor comprising: a substrate, (Murakami et al. Figure 1 #1), comprising a well region of a first conductivity type, (Murakami et al. Figure 1 #20); a field oxide layer, (Murakami et al. Figure 1 #15), located over the well region, (Murakami et al. Figure 1 #20); a first source region of a second conductivity type, (Murakami et al. Figure 1 #9), and a first drain region of a second conductivity type, (Murakami et al. Figure 1 #9), separated by the field oxide layer, (Murakami et al. Figure 1 #15); a second source region having a second conductivity type, (Murakami et al. Figure 1 #7), concentration lower than the first source region, (Murakami et al. Figure 1 #9), the second source region, (Murakami et al. Figure 1 #7), formed in the well region, (Murakami et al. Figure 1 #20), adjacent the first source region, (Murakami et al. Figure 1 #9), with a portion of the second source region, (Murakami et al. Figure 1 #7), underlying the field oxide layer,

(Murakami et al. Figure 1 #15); a second drain region having a second conductivity type, (Murakami et al. Figure 1 #7), concentration lower than the first drain region, (Murakami et al. Figure 1 #9), the second drain region formed, (Murakami et al. Figure 1 #7), in the well region, (Murakami et al. Figure 1 #20), adjacent the first drain region, (Murakami et al. Figure 1 #9), with a portion of the second drain region, (Murakami et al. Figure 1 #7), underlying the field oxide layer, (Murakami et al. Figure 1 #15); and a conductive layer, (Murakami et al. Figure 1 #17), formed over the field oxide layer, (Murakami et al. Figure 1 #15), the conductive layer, (Murakami et al. Figure 1 #17), overlapping the second source region, (Murakami et al. Figure 1 #7), and the second drain region, (Murakami et al. Figure 1 #7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 19, 27, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art.

8. Referring to claim 1, a field transistor comprising: a well region of a first conductivity type, (Applicant's Admitted Prior Art Figure 1 #13); a field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17), for defining an active region, (Applicant's Admitted Prior Art Figure 1 in the area of #13 under the gate #18), on the well region, (Applicant's Admitted Prior Art Figure

1 #13); high concentration source, (Applicant's Prior Art Figure 1 #14), and drain regions of a second conductivity type, (Applicant's Prior Art Figure 1 #15), separated from each other by a width of the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17); a low concentration source region of the second conductivity type, (See * below), formed in the well region, (Applicant's Admitted Prior Art Figure 1 #13), the low concentration source, (See * below), region being adjacent to the high concentration source region, (Applicant's Prior Art Figure 1 #14), and overlapped by one end of the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17); a low concentration drain region of the second conductivity type, (See * below), formed in the well region, (Applicant's Admitted Prior Art Figure 1 #13), the low concentration drain region, (See * below), being adjacent to the high concentration drain region, (Applicant's Prior Art Figure 1 #15), and overlapped by the other end of the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17); and a gate conductive layer pattern, (Applicant's Admitted Prior Art Figure 1 #18), formed on the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17), the gate conductive layer pattern, (Applicant's Admitted Prior Art Figure 1 #18), overlapping parts of the low concentration source and drain regions of the second conductivity type, (See * below).

* The Applicant's admitted prior art also teaches the claimed matter in claim 1. The Applicant's Prior art in Figure 1 shows the n+ source and drain region #s 14 and 15 under the FOX layer 17. The areas, which are directly under the Fox layer 17 are labeled by the examiner in the color of red and they represent the areas of the claimed LDD. It is apparent that these areas have less dopant concentration than the areas that are color green in the source and drain. The processing steps would actually build the structure in Figure 1 to have the LDD due to the

fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

9. Referring to claim 19, a semiconductor device, comprising: a substrate, (Applicant's Admitted Prior Art Figure 1 #11), comprising a well region of a first conductivity type, (Applicant's Admitted Prior Art Figure 1 #13); a field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17), located over a portion of the well region, (Applicant's Admitted Prior Art Figure 1 #13); a first source region of a second conductivity type, (Applicant's Prior Art Figure 1 #14), and a first drain region of a second conductivity type, (Applicant's Prior Art Figure 1 #15), separated by the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17); a second source region having a second conductivity type concentration lower, (See * below), than the first source region, (Applicant's Prior Art Figure 1 #14), the second source region, (See * below), formed in the well region, (Applicant's Admitted Prior Art Figure 1 #13), adjacent the first source region, (Applicant's Prior Art Figure 1 #14), with a portion of the second source region, (See * below), underlying the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17); a second drain region having a second conductivity type concentration lower, (See * below), than the first drain region, (Applicant's Prior Art Figure 1 #15), the second drain region, (See * below), formed in the well region, (Applicant's Admitted Prior Art Figure 1 #13), adjacent the first drain region, (Applicant's Prior Art Figure 1 #15), with a portion of the second drain region, (See * below), underlying the field oxide layer, (Applicant's Admitted Prior Art); and a conductive layer, (Applicant's Admitted Prior Art Figure 1 #18), formed over the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17), the conductive layer, (Applicant's

Admitted Prior Art Figure 1 #18), overlapping the second source region, (See * below), and the second drain region, (See * below).

* The Applicant's admitted prior art also teaches the claimed matter in claim 19. The Applicant's Prior art in Figure 1 shows the n+ source and drain region #s 14 and 15 under the FOX layer 17. The areas, which are directly under the Fox layer 17 are labeled by the examiner in the color of red and they represent the areas of the claimed LDD. It is apparent that these areas have less dopant concentration than the areas that are color green in the source and drain. The processing steps would actually build the structure in Figure 1 to have the LDD due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

10. Referring to claim 27, a semiconductor device comprising: a substrate, (Applicant's Admitted Prior Art Figure 1 #11), comprising a well region of a first conductivity type, (Applicant's Admitted Prior Art Figure 1 #13); a field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17), located over the well region, (Applicant's Admitted Prior Art Figure 1 #13); a first source region of a second conductivity type, (Applicant's Prior Art Figure 1 #14), and a first drain region of a second conductivity type, (Applicant's Prior Art Figure 1 #15), separated by the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17); a second source region having a second conductivity type, (See * below), concentration lower than the first source region, (Applicant's Prior Art Figure 1 #14), the second source region, (See * below), formed in the well region, (Applicant's Admitted Prior Art Figure 1 #13), adjacent the first source region, (Applicant's Prior Art Figure 1 #14), with a portion of the second source region, (See * below), underlying the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17); a second drain

region having a second conductivity type, (See * below), concentration lower than the first drain region, (Applicant's Prior Art Figure 1 #15), the second drain region, (See * below), formed in the well region, (Applicant's Admitted Prior Art Figure 1 #13), adjacent the first drain region, (Applicant's Prior Art Figure 1 #15), with a portion of the second drain region underlying the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17); a conductive layer formed over the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17), the conductive layer, (Applicant's Admitted Prior Art Figure 1 #18), overlapping the second source region, (See * below), and the second drain region, (See * below); a gate electrode, (Applicant's Admitted Prior Art Figure 1 #20), electrically connected to the conductive layer, (Applicant's Admitted Prior Art Figure 1 #18); a source electrode, (Applicant's Admitted Prior Art Figure 1 #21), electrically connected to the first source region, (Applicant's Prior Art Figure 1 #14); and a drain electrode, (Applicant's Admitted Prior Art Figure 1 #22), electrically connected to the first drain region, (Applicant's Prior Art Figure 1 #15).

* The Applicant's admitted prior art also teaches the claimed matter in claim 27. The Applicant's Prior art in Figure 1 shows the n+ source and drain region #s 14 and 15 under the FOX layer 17. The areas, which are directly under the Fox layer 17 are labeled by the examiner in the color of red and they represent the areas of the claimed LDD. It is apparent that these areas have less dopant concentration than the areas that are color green in the source and drain. The processing steps would actually build the structure in Figure 1 to have the LDD due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

11. Referring to claim 29, a system for electrostatic discharge protection containing a field transistor comprising: a substrate, (Applicant's Admitted Prior Art Figure 1 #11), comprising a well region of a first conductivity type, (Applicant's Admitted Prior Art Figure 1 #13); a field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17), located over the well region, (Applicant's Admitted Prior Art Figure 1 #13); a first source region of a second conductivity type, (Applicant's Prior Art Figure 1 #14), and a first drain region of a second conductivity type, (Applicant's Prior Art Figure 1 #15), separated by the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17); a second source region having a second conductivity type, (See * below), concentration lower than the first source region, (Applicant's Prior Art Figure 1 #14), the second source region, (See * below), formed in the well region, (Applicant's Admitted Prior Art Figure 1 #13), adjacent the first source region, (Applicant's Prior Art Figure 1 #14), with a portion of the second source region, (See * below), underlying the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17); a second drain region having a second conductivity type, (See * below), concentration lower than the first drain region, (Applicant's Prior Art Figure 1 #15), the second drain region formed, (See * below), in the well region, (Applicant's Admitted Prior Art Figure 1 #13), adjacent the first drain region, (Applicant's Prior Art Figure 1 #15), with a portion of the second drain region, (See * below), underlying the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17); and a conductive layer, (Applicant's Admitted Prior Art Figure 1 #18), formed over the field oxide layer, (Applicant's Admitted Prior Art Figure 1 #17), the conductive layer, (Applicant's Admitted Prior Art Figure 1 #18), overlapping the second source region, (See * below), and the second drain region, (See * below).

* The Applicant's admitted prior art also teaches the claimed matter in claim 29. The Applicant's Prior art in Figure 1 shows the n+ source and drain region #s 14 and 15 under the FOX layer 17. The areas, which are directly under the Fox layer 17 are labeled by the examiner in the color of red and they represent the areas of the claimed LDD. It is apparent that these areas have less dopant concentration than the areas that are color green in the source and drain. The processing steps would actually build the structure in Figure 1 to have the LDD due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art in view of U.S. Patent No. 5,623,154 Murakami et al.

12. Referring to claim 2, a field transistor, wherein the well region of the first conductivity type, (Applicant's Admitted Prior Art Figure 1 #13 & Murakami et al. Figure 1 #20), is formed on a high concentration buried region of the first conductivity type, (Applicant's Admitted Prior Art Figure 1 #12 & Murakami et al. Figure 1 #3), on a semiconductor substrate of the first conductivity type, (Applicant's Admitted Prior Art Figure 1 #11 & Murakami et al. Figure 1 #1).

It would have been obvious to one skilled in the art to combine the teachings of the Applicant's Admitted Prior Art with the teachings of Murakami et al. because the LDD structure is effective to relax a field intensity in channel direction near the drain region, and hence to suppress the generation of hot electrons, (Murakami et al. Col. 1 Lines 34-37).

13. Referring to claim 3, a field transistor, wherein the well region of the first conductivity type is formed on a semiconductor substrate of the second conductivity type.

Applicant's Admitted Prior Art discloses the claimed invention except for second conductive type substrate. It would have been obvious to one having

ordinary skill in the art at the time the invention was made to make the substrate out of a second conductive type material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ

416.

14. Referring to claim 4, a field transistor, further comprising a high concentration diffusion region of the first conductivity type, (Applicant's Admitted Prior Art Figure 1 #16), formed in the well region, (Applicant's Admitted Prior Art Figure 1 #13 & Murakami et al. Figure 1 #20), the high concentration diffusion region, (Applicant's Admitted Prior Art Figure 1 #16), being separated from the high concentration source region of the second conductive type, (Applicant's Admitted Prior Art and Murakami et al. Figure 1 #9), by a predetermined distance.

15. Referring to claim 5, a field transistor, further comprising a low concentration diffusion region of the first conductivity type, (Applicant's Admitted Prior Art Figure 1 Examiner labeled yellow & see ** below), and a low concentration diffusion region of the second conductivity

type, (Applicant's Admitted Prior Art Figure 1 Examiner labeled orange & see *** below), both low concentration diffusion regions being adjacent to each other between the high concentration diffusion region of the first conductivity type, (Applicant's Admitted Prior Art Figure 1 #16), and the high concentration source region of the second conductivity type, (Applicant's Admitted Prior Art Figure 1 #14 and Murakami et al. Figure 1 #9).

** The Applicant's admitted prior art also teaches the claimed matter in claim 5. The Applicant's Prior art in Figure 1 shows the p+ diffusion region # 16 under the FOX layer 17. The area, which is directly under the Fox layer 17 is labeled by the examiner in the color of yellow and they represent the areas of the claimed low dopant concentration of the first conductivity. It is apparent that this area has less dopant concentration than the area that is color purple in the diffusion region. The processing steps would actually build the structure in Figure 1 to have the low dopant concentration of the first conductivity diffusion region due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

*** The Applicant's admitted prior art also teaches the claimed matter in claim 5. The Applicant's Prior art in Figure 1 shows the n+ source region # 14 under the FOX layer 17. The area, which is directly under the Fox layer 17 is labeled by the examiner in the color of orange and they represent the areas of the claimed low dopant concentration of the second conductivity. It is apparent that this area has less dopant concentration than the area that is color green in the source. The processing steps would actually build the structure in Figure 1 to have the low dopant concentration of the second conductivity diffusion region due to the fact that the dopant

concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

16. Referring to claim 6, a field transistor, wherein the low concentration diffusion region of the first conductivity type, (Applicant's Admitted Prior Art Figure 1 Examiner labeled yellow & see ** below), is adjacent to the high concentration diffusion region of the first conductivity type, (Applicant's Admitted Prior Art Figure 1 #16), and the low concentration diffusion region of the second conductivity type, (Applicant's Admitted Prior Art Figure 1 Examiner labeled orange & see *** below), is adjacent to the high concentration source region of the second conductivity type, (Applicant's Admitted Prior Art Figure 1 #14 and Murakami et al. Figure 1 #9).

** The Applicant's admitted prior art also teaches the claimed matter in claim 6. The Applicant's Prior art in Figure 1 shows the p+ diffusion region # 16 under the FOX layer 17. The area, which is directly under the Fox layer 17 is labeled by the examiner in the color of yellow and they represent the areas of the claimed low dopant concentration of the first conductivity. It is apparent that this area has less dopant concentration than the area that is color purple in the diffusion region. The processing steps would actually build the structure in Figure 1 to have the low dopant concentration of the first conductivity diffusion region due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

*** The Applicant's admitted prior art also teaches the claimed matter in claim 6. The Applicant's Prior art in Figure 1 shows the n+ source region # 14 under the FOX layer 17. The area, which is directly under the Fox layer 17 is labeled by the examiner in the color of orange

and they represent the areas of the claimed low dopant concentration of the second conductivity. It is apparent that this area has less dopant concentration than the area that is color green in the source. The processing steps would actually build the structure in Figure 1 to have the low dopant concentration of the second conductivity diffusion region due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

17. Referring to claim 7, a field transistor, further comprising: a gate electrode, (Applicant's Admitted Prior Art Figure 1 #20), electrically connected to the gate conductive layer pattern, (Applicant's Admitted Prior Art Figure 1 #18); a source electrode, (Applicant's Admitted Prior Art Figure 1 #21), electrically connected to the high concentration source region of the second conductivity type, (Applicant's Admitted Prior Art Figure 1 #14); and a drain electrode, (Applicant's Admitted Prior Art Figure 1 #22), electrically connected to the high concentration drain region of the second conductivity type, (Applicant's Admitted Prior Art Figure 1 #15).

18. Referring to claim 8, a field transistor, wherein the drain electrode, (Applicant's Admitted Prior Art Figure 1 #22), is electrically connected to the gate electrode, (Applicant's Admitted Prior Art Figure 1 #20).

19. Referring to claim 9, a field transistor, wherein the source electrode, (Applicant's Admitted Prior Art Figure 1 #21), is electrically connected to the high concentration diffusion region of the first conductivity type as well, (Applicant's Admitted Prior Art Figure 1 #16).

20. Referring to claim 10, a field transistor, wherein the first conductivity type is p-type, and the second conductivity type is n-type, (Applicant's Admitted Prior Art Figure 1).

20. Referring to claim 20, a semiconductor device, further comprising a first diffusion region of the first conductivity type, (Applicant's Admitted Prior Art Figure 1 #16), formed in the well region, (Applicant's Admitted Prior Art Figure 1 #13 & Murakami et al. Figure 1 #20), and separated from the first source region, (Applicant's Prior Art Figure 1 #14 & Murakami et al. Figure 1 #9).

It would have been obvious to one skilled in the art to combine the teachings of the Applicant's Admitted Prior Art with the teachings of Murakami et al. because the LDD structure is effective to relax a field intensity in channel direction near the drain region, and hence to suppress the generation of hot electrons, (Murakami et al. Col. 1 Lines 34-37).

21. Referring to claim 21, a semiconductor device, further comprising a second diffusion region having a first conductivity type, (Applicant's Admitted Prior Art Figure 1 Examiner labeled yellow & see ** below), concentration lower than the first diffusion region, (Applicant's Admitted Prior Art Figure 1 #16), and comprising a third diffusion region of the second conductivity type, (Applicant's Admitted Prior Art Figure 1 Examiner labeled orange & see *** below), both the second, (Applicant's Admitted Prior Art Figure 1 Examiner labeled yellow & see ** below), and third diffusion regions, (Applicant's Admitted Prior Art Figure 1 Examiner labeled orange & see *** below), adjacent each other and located between the first diffusion region, (Applicant's Admitted Prior Art Figure 1 #16), and the first source region, (Applicant's Prior Art Figure 1 #14 & Murakami et al. Figure 1 #9).

** The Applicant's admitted prior art also teaches the claimed matter in claim 6. The Applicant's Prior art in Figure 1 shows the p+ diffusion region # 16 under the FOX layer 17. The area, which is directly under the Fox layer 17 is labeled by the examiner in the color of

yellow and they represent the areas of the claimed low dopant concentration of the first conductivity. It is apparent that this area has less dopant concentration than the area that is color purple in the diffusion region. The processing steps would actually build the structure in Figure 1 to have the low dopant concentration of the first conductivity diffusion region due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

*** The Applicant's admitted prior art also teaches the claimed matter in claim 6. The Applicant's Prior art in Figure 1 shows the n+ source region # 14 under the FOX layer 17. The area, which is directly under the Fox layer 17 is labeled by the examiner in the color of orange and they represent the areas of the claimed low dopant concentration of the second conductivity. It is apparent that this area has less dopant concentration than the area that is color green in the source. The processing steps would actually build the structure in Figure 1 to have the low dopant concentration of the second conductivity diffusion region due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

22. Referring to claim 22, a semiconductor device, the second diffusion region type, (Applicant's Admitted Prior Art Figure 1 Examiner labeled yellow & see ** below), located adjacent the first diffusion region, (Applicant's Admitted Prior Art Figure 1 #16), and the third diffusion region, (Applicant's Admitted Prior Art Figure 1 Examiner labeled orange & see *** below), located adjacent the first source region, (Applicant's Prior Art Figure 1 #14 & Murakami et al. Figure 1 #9).

** The Applicant's admitted prior art also teaches the claimed matter in claim 6. The Applicant's Prior art in Figure 1 shows the p+ diffusion region # 16 under the FOX layer 17. The area, which is directly under the Fox layer 17 is labeled by the examiner in the color of yellow and they represent the areas of the claimed low dopant concentration of the first conductivity. It is apparent that this area has less dopant concentration than the area that is color purple in the diffusion region. The processing steps would actually build the structure in Figure 1 to have the low dopant concentration of the first conductivity diffusion region due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

*** The Applicant's admitted prior art also teaches the claimed matter in claim 6. The Applicant's Prior art in Figure 1 shows the n+ source region # 14 under the FOX layer 17. The area, which is directly under the Fox layer 17 is labeled by the examiner in the color of orange and they represent the areas of the claimed low dopant concentration of the second conductivity. It is apparent that this area has less dopant concentration than the area that is color green in the source. The processing steps would actually build the structure in Figure 1 to have the low dopant concentration of the second conductivity diffusion region due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

23. Referring to claim 23, a semiconductor device, further comprising: a gate electrode, (Applicant's Admitted Prior Art Figure 1 #20), electrically connected to the conductive layer, (Applicant's Admitted Prior Art Figure 1 #18); a source electrode, (Applicant's Admitted Prior Art Figure 1 #21), electrically connected to the first source region, (Applicant's Admitted Prior

Art Figure 1 #14); and a drain electrode, (Applicant's Admitted Prior Art Figure 1 #22), electrically connected to the first drain region, (Applicant's Admitted Prior Art Figure 1 #15).

24. Referring to claim 24, a semiconductor device, wherein the drain electrode, (Applicant's Admitted Prior Art Figure 1 #22), being electrically connected to the gate electrode, (Applicant's Admitted Prior Art Figure 1 #20).

25. Referring to claim 25, a semiconductor device, wherein the source electrode, (Applicant's Admitted Prior Art Figure 1 #21), being electrically connected to the first diffusion region, (Applicant's Admitted Prior Art Figure 1 #16).

26. Referring to claim 26, a semiconductor device, wherein the first conductivity type is p-type and the second conductivity type is n-type, (Applicant's Admitted Prior Art Figure 1).

27. Referring to claim 28, a semiconductor device, further comprising a first diffusion region of the first conductivity type, (Applicant's Admitted Prior Art Figure 1 #16), formed in the well region, (Applicant's Prior Art Figure 1 #13 & Murakami et al. Figure 1 #20), and separated from the first source region, (Applicant's Prior Art Figure 1 #14 & Murakami et al. Figure 1 #9), a second diffusion region having a first conductivity type, (Applicant's Admitted Prior Art Figure 1 Examiner labeled yellow & see ** below), concentration lower than the first diffusion region, (Applicant's Admitted Prior Art Figure 1 #16), and a third diffusion region of the second conductivity type, (Applicant's Admitted Prior Art Figure 1 Examiner labeled orange & see *** below), wherein both the second, (Applicant's Admitted Prior Art Figure 1 Examiner labeled yellow & see ** below), and third diffusion regions, (Applicant's Admitted Prior Art Figure 1 Examiner labeled orange & see *** below), are adjacent each other and located between the first

diffusion region, (Applicant's Admitted Prior Art Figure 1 #16), and the first source region, (Applicant's Prior Art Figure 1 #14 & Murakami et al. Figure 1 #9).

** The Applicant's admitted prior art also teaches the claimed matter in claim 6. The Applicant's Prior art in Figure 1 shows the p+ diffusion region # 16 under the FOX layer 17. The area, which is directly under the Fox layer 17 is labeled by the examiner in the color of yellow and they represent the areas of the claimed low dopant concentration of the first conductivity. It is apparent that this area has less dopant concentration than the area that is color purple in the diffusion region. The processing steps would actually build the structure in Figure 1 to have the low dopant concentration of the first conductivity diffusion region due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

*** The Applicant's admitted prior art also teaches the claimed matter in claim 6. The Applicant's Prior art in Figure 1 shows the n+ source region # 14 under the FOX layer 17. The area, which is directly under the Fox layer 17 is labeled by the examiner in the color of orange and they represent the areas of the claimed low dopant concentration of the second conductivity. It is apparent that this area has less dopant concentration than the area that is color green in the source. The processing steps would actually build the structure in Figure 1 to have the low dopant concentration of the second conductivity diffusion region due to the fact that the dopant concentration is always higher at the top of the layer than the bottom and the FOX layer serves as a mask.

References

28. U.S. Patent No. 6,359,318 was not used in this action, but is noted for Applicant's consideration in regard to the diffusion regions of the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
December 11, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800